

PROGRAM: B.Tech.-Electronics

SEMESTER: 4

TIMETABLE-Section A

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECCEC405R01-A	BECCEC405R01-A	BECCEC405R01-A	BECDEC402-A	BECCEC405R01-A	BECCEC403R01-A		BECCTP407R01-A			
Tue	BECCEC406R01-A	BECCEC406R01-A	BECCEC406R01-A		BECDECE401-A		BECCEC405R01-A	BECCEC405R01-A	BECCEC405R01-A		
Wed	BECCEC402R01-A	BECCEC404R01-A	BECCEC403R01-A	BECDEC401-A		BECCEC404R01-A	BECCEC404R01-A	BECCEC406R01-A	BECCEC406R01-A	BECCEC406R01-A	
Thu	BECCEC403R01-A	BECCEC403R01-A		BECCEC405R01-A	BECCEC405R01-A	BECCEC405R01-A		BECDECE402-A	BECCEC402R01-A		
Fri	BECDEC402-A	BECDEC401-A	BECCEC404R01-A	BECCEC406R01-A	BECCEC406R01-A	BECCEC406R01-A					
Sat				BECCEC404R01-A		BECCEC402R01-A	BECCEC403R01-A		BECDEC402-A		

	Code	Description	Section	Faculty	Venue
	BECCEC402R01	NETWORK THEORY	A	Ramya, R	VV204, VIDHYUTH VIHAR
	BECCEC403R01	LINEAR INTEGRATED CIRCUITS	A	Easwaran, M	VV204, VIDHYUTH VIHAR
	BECCEC404R01	SIGNALS AND SYSTEMS	A	Jayabharathy, R	VV204, VIDHYUTH VIHAR
	BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	A	Ramya, R	LAB, VIDHYUTH VIHAR
	BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	A	Raghupathi, S	LAB, VIDHYUTH VIHAR
	BECCEC401R01	DISCRETE MATHEMATICS	A	Venkatakrishnan, Y B	VV204, VIDHYUTH VIHAR
	BECCTP407R01	HR SKILLS	A	Seema, S	GNV101, GNANA VIHAR
	BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	A	Suganthi, G	VV204, VIDHYUTH VIHAR
	BECDEC402	CONTROL ENGINEERING	A	Madhava Sarma, P	VV204, VIDHYUTH VIHAR

TIMETABLE-Section B

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECCEC403R01-B	BECCEC404R01-B	BECCEC404R01-B	BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B		BECCEC403R01-B	BECCEC402R01-B		
Tue	BECCEC406R01-B	BECCEC406R01-B	BECCEC406R01-B		BECCEC406R01-B	BECCEC406R01-B					
Wed	BECCEC403R01-B	BECCEC402R01-B	BECCEC401-B		BECCEC403R01-B	BECCEC403R01-B	BECCEC404R01-B	BECCEC404R01-B	BECCEC404R01-B	BECCEC401-B	
Thu	BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B	BECCEC404R01-B	BECCEC402R01-B			BECDECE402-B		
Fri	BECCEC406R01-B	BECCEC406R01-B	BECCEC406R01-B		BECDEC402-B		BECDEC401-B	BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B	
Sat	BECCEC404R01-B	BECCEC402R01-B		BECDEC402-B		BECDEC401-B	BECCEC406R01-B	BECCEC406R01-B	BECCEC406R01-B		
	BECDEC401-B	BECCEC403R01-B	BECDEC402-B	BECCEC402R01-B	BECCEC402R01-B	BECCEC402R01-B	BECCEC403R01-B	BECCEC403R01-B	BECCEC403R01-B	BECCEC403R01-B	

	Code	Description	Section	Faculty	Venue
	BECCEC402R01	NETWORK THEORY	B	Ramya, R	VV205, VIDHYUTH VIHAR
	BECCEC403R01	LINEAR INTEGRATED CIRCUITS	B	Parvathy, A	VV205, VIDHYUTH VIHAR
	BECCEC404R01	SIGNALS AND SYSTEMS	B	Narasimhan, K	VV205, VIDHYUTH VIHAR
	BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	B	Raju, N	LAB, VIDHYUTH VIHAR
	BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	B	Parvathy, A	LAB, VIDHYUTH VIHAR
	BECCEC401R01	DISCRETE MATHEMATICS	B	Balaji, S	VV205, VIDHYUTH VIHAR
	BECCTP407R01	HR SKILLS	B	Chandrasekar, V	GNV101, GNANA VIHAR
	BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	B	Nimma Jegadeesan	VV205, VIDHYUTH VIHAR
	BECDEC402	CONTROL ENGINEERING	B	Madhava Sarma, P	VV205, VIDHYUTH VIHAR

TIMETABLE-Section C

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECDEC402-C	BECDEC401-C	BECCEC401R01-C	BECCEC404R01-C	BECCEC403R01-C		BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C		
Tue	BECCEC406R01-C	BECCEC406R01-C	BECCEC406R01-C		BECCEC406R01-C	BECCEC406R01-C					
Wed	BECCEC403R01-C	BECCEC402R01-C	BECDEC402-C		BECCEC403R01-C	BECCEC403R01-C	BECCEC404R01-C	BECCEC404R01-C	BECCEC402R01-C	BECCEC402R01-C	
Thu	BECDEC402-C	BECCEC402R01-C	BECDEC401-C	BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C			BECCEC403R01-C		
Fri	BECCEC406R01-C	BECCEC406R01-C	BECCEC406R01-C		BECCEC406R01-C	BECCEC406R01-C					
Sat	BECCEC404R01-C	BECCEC403R01-C		BECDEC402-C	BECCEC404R01-C		BECCTP407R01-C	BECCEC404R01-C	BECCEC404R01-C	BECCEC404R01-C	
	BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C	BECCEC402R01-C		BECCEC404R01-C		BECDEC401-C		

	Code	Description	Section	Faculty	Venue
	BECCEC402R01	NETWORK THEORY	C	Priyadharshini, S	VV206, VIDHYUTH VIHAR
	BECCEC403R01	LINEAR INTEGRATED CIRCUITS	C	Har Narayan Upadhyay	VV206, VIDHYUTH VIHAR
	BECCEC404R01	SIGNALS AND SYSTEMS	C	Ananthan, T	VV206, VIDHYUTH VIHAR
	BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	C	Avi, J	LAB, VIDHYUTH VIHAR

BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	C	Priyadharshini, S	LAB, VIDHYUTH VIHAR
BECMA401R01	DISCRETE MATHEMATICS	C	Seethalakshmi, R	VV206, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS	C	Balaji, K	GNV101, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	C	Devasena, L	VV206, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	C	Jayalalitha, S	VV206, VIDHYUTH VIHAR

TIMETABLE-Section D

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECDEC402-D	BECCEC402R01-D		BECCEC404R01-D		BECMA401R01-D	BECCEC403R01-D	BECDEC401-D			
Tue	BECCEC405R01-D	BECCEC405R01-D	BECCEC405R01-D	BECMA401R01-D	BECCEC403R01-D	BECCEC404R01-D			BECCEC402R01-D		
Wed	BECDEC401-D	BECMA401R01-D	BECCEC403R01-D	BECDEC402-D			BECCEC405R01-D	BECCEC405R01-D	BECCEC405R01-D		
Thu	BECCTP407R01-D	BECDEC401-D	BECMA401R01-D	BECCEC402R01-D		BECCEC404R01-D	BECCEC402R01-D	BECCEC403R01-D	BECDEC402-D		
Fri	BECDEC402-D	BECDEC401-D		BECCEC405R01-D	BECCEC405R01-D	BECCEC405R01-D		BECCEC404R01-D	BECMA401R01-D		
Sat				BECCEC406R01-D	BECCEC406R01-D	BECCEC406R01-D					

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	D	Jayabharathy, R	VV213, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	D	Har Narayan Upadhyay	VV213, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	D	Narasimhan, K	VV213, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	D	Sundararaman, R	LAB, VIDHYUTH VIHAR
BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	D	Narasimhan, K	LAB, VIDHYUTH VIHAR
BECMA401R01	DISCRETE MATHEMATICS	D	Krishnakumari, B	VV213, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS	D	Balakothandapani, S	GNV101, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	D	Devasena, L	VV213, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	D	Sainabha, M	VV213, VIDHYUTH VIHAR

TIMETABLE-Section E

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECDEC402-E	BECCEC403R01-E		BECCEC402R01-E		BECCEC404R01-E	BECDEC401-E	BECCEC402R01-E			
Tue	BECMA401R01-E	BECDEC402-E	BECCEC402R01-E	BECCEC405R01-E	BECCEC405R01-E	BECCEC405R01-E			BECCEC404R01-E		
Wed	BECCEC403R01-E	BECDEC401-E	BECMA401R01-E	BECCEC404R01-E			BECCEC404R01-E	BECMA401R01-E	BECCTP407R01-E		
Thu	BECCEC405R01-E	BECCEC405R01-E	BECCEC405R01-E	BECDEC401-E	BECMA401R01-E	BECCEC403R01-E		BECDEC402-E	BECCEC403R01-E		
Fri	BECCEC406R01-E	BECCEC406R01-E	BECCEC406R01-E				BECCEC405R01-E	BECCEC405R01-E	BECCEC405R01-E		
Sat	BECCEC402R01-E	BECDEC402-E		BECDEC401-E	BECMA401R01-E		BECCEC406R01-E	BECCEC406R01-E	BECCEC406R01-E		

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	E	Jayabharathy, R	VV214, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	E	Easwaran, M	VV214, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	E	Ananthan, T	VV214, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	E	Jayabharathy, R	LAB, VIDHYUTH VIHAR
BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	E	Raajan, N R	LAB, VIDHYUTH VIHAR
BECMA401R01	DISCRETE MATHEMATICS	E	Natarajan, C	VV214, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS	E	Krishnamurthy, A V	GNV101, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	E	Nimula Jegadeesan	VV214, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	E	Sumathi, J	VV214, VIDHYUTH VIHAR