

PROGRAM: B.Tech.-Electronics & Communication Engineering

SEMESTER: 4

TIMETABLE-Section A

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECCEC405R01-A	BECCEC405R01-A	BECCEC405R01-A	BECDEC402-A		BECCEC404R01-A	BECCEC403R01-A	BECCEC403R01-A	BECCEC401-A		
Tue	BECCEC406R01-A	BECCEC406R01-A	BECCEC406R01-A	BECCEC404R01-A	BECCEC402R01-A		BECCEC405R01-A	BECCEC405R01-A	BECCEC405R01-A		
Wed	BECCEC402R01-A	BECCEC404R01-A		BECCEC404R01-A		BECCEC403R01-A	BECCEC402-A	BECCEC406R01-A	BECCEC406R01-A	BECCEC406R01-A	
Thu	BECCEC402R01-A	BECCEC404R01-A	BECCEC402R01-A	BECCEC405R01-A	BECCEC405R01-A	BECCEC405R01-A		BECCEC403R01-A			
Fri	BECCEC403R01-A	BECCEC402R01-A	BECCEC404R01-A	BECCEC406R01-A	BECCEC406R01-A	BECCEC406R01-A	BECCEC402-A	BECCEC403R01-A			
Sat											

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	A	Padma Priya, V	VV316, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	A	Susan, D	VV316, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	A	John Bosco Balaguru, R	VV316, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	A	Avila, J	LAB, VIDHYUTH VIHAR
BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	A	Susan, D	LAB, VIDHYUTH VIHAR
BECCEC401R01	DISCRETE MATHEMATICS	A	Balaji, S	VV316, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS - II	A	Chandrasekar, V	GNV205, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	A	Avila, J	VV316, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	A	Venkatesh, S	VV316, VIDHYUTH VIHAR

TIMETABLE-Section B

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon		BECCEC403R01-B	BECCEC403R01-B	BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B		BECDEC402-B	BECCEC404R01-B		
Tue		BECCEC402R01-B	BECCEC403R01-B	BECCEC406R01-B	BECCEC406R01-B	BECCEC406R01-B		BECCEC404R01-B	BECCEC401-B		
Wed		BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B	BECCEC402R01-B	BECCEC403R01-B	BECCEC402-B		BECCEC401-B		
Thu		BECCEC406R01-B	BECCEC406R01-B	BECCEC406R01-B				BECCEC405R01-B	BECCEC405R01-B	BECCEC405R01-B	
Fri	BECCTP407R01-B	BECCEC402-B	BECCEC404R01-B	BECCEC401-B	BECCEC402R01-B		BECCEC406R01-B	BECCEC406R01-B	BECCEC406R01-B		
Sat											

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	B	Viswanathan, B	VV205, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	B	Wilson, K J	VV205, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	B	Balu, R	VV205, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	B	Lakshmi, C	LAB, VIDHYUTH VIHAR
BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	B	Prasath, R K	LAB, VIDHYUTH VIHAR
BECCEC401R01	DISCRETE MATHEMATICS	B	Natarajan, C	VV205, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS - II	B	Brinda Kailash Giri	GNV311, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	B	Jeyaprakash, B G	VV205, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	B	Manigandan, N S	VV205, VIDHYUTH VIHAR

TIMETABLE-Section C

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon		BECCEC404R01-C	BECDEC401-C	BECCEC404R01-C	BECDEC402-C		BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C		
Tue		BECCEC402R01-C	BECDEC402-C	BECCEC404R01-C		BECCEC403R01-C	BECCEC406R01-C	BECCEC406R01-C	BECCEC406R01-C		
Wed		BECCEC402R01-C	BECCEC403R01-C	BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C		BECCEC402-C			
Thu	BECDEC402-C	BECCEC403R01-C	BECCEC402R01-C	BECCEC406R01-C	BECCEC406R01-C	BECCEC406R01-C	BECCEC404R01-C	BECCEC404R01-C	BECCEC401-C	BECCTP407R01-C	
Fri	BECCEC405R01-C	BECCEC405R01-C	BECCEC405R01-C	BECCEC403R01-C	BECCEC406R01-C	BECCEC406R01-C	BECCEC402R01-C	BECCEC404R01-C			
Sat											

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	C	Susan, D	VV206, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	C	Wilson, K J	VV206, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	C	Chandrasekar, N	VV206, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	C	Jaiseeli, C	LAB, VIDHYUTH VIHAR

BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	C	Asokan, J	LAB, VIDHYUTH VIHAR
BECCEC401R01	DISCRETE MATHEMATICS	C	Balaji, S	VV206, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS - II	C	Ravi, R	GNV313, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	C	Asokan, J	VV206, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	C	Venkatesh, S	VV206, VIDHYUTH VIHAR

TIMETABLE-Section D

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECDEC402-D	BECCEC402R01-D	BECDEC401-D	BECCEC404R01-D		BECCEC403R01-D	BECCEC401R01-D	BECCTP407R01-D	BECCEC404R01-D		
	BECCEC405R01-D	BECCEC405R01-D	BECCEC405R01-D	BECCEC401R01-D		BECDEC401-D	BECCEC402R01-D	BECCEC403R01-D			
Tue	BECCEC406R01-D	BECCEC406R01-D	BECCEC406R01-D								
		BECCEC401R01-D	BECDEC401-D	BECCEC404R01-D	BECDEC402-D		BECCEC405R01-D	BECCEC405R01-D	BECCEC405R01-D		
Wed							BECCEC406R01-D	BECCEC406R01-D	BECCEC406R01-D		
Thu	BECCEC401R01-D	BECCEC402R01-D	BECDEC402-D	BECDEC401-D		BECCEC403R01-D		BECCEC404R01-D			
		BECCEC402R01-D	BECCEC403R01-D	BECCEC405R01-D	BECCEC405R01-D	BECCEC405R01-D		BECDEC402-D	BECCEC401R01-D		
Fri				BECCEC406R01-D	BECCEC406R01-D	BECCEC406R01-D					
Sat											

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	D	Lakshmi, C	VV213, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	D	Rakesh Kumar Karn	VV213, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	D	Raj Kumar, G	VV213, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	D	Raj Kumar, G	LAB, VIDHYUTH VIHAR
BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	D	Balu, R	LAB, VIDHYUTH VIHAR
BECCEC401R01	DISCRETE MATHEMATICS	D	Rajaraman, R	VV213, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS - II	D	Chandrasekar, V	GNV205, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	D	Chandrasekar, M	VV213, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	D	Gomathi, V	VV213, VIDHYUTH VIHAR

TIMETABLE-Section E

	I	II	III	IV	V	VI	VII	VIII	IX	X	XI
	08:40-09:30	09:30-10:20	10:20-11:10	11:30-12:20	12:20-13:10	13:10-14:00	14:20-15:10	15:10-16:00	16:00-16:50	17:00-17:50	17:50-18:40
Mon	BECCEC403R01-E	BECCEC402R01-E	BECDEC401-E	BECCTP407R01-E		BECCEC404R01-E	BECDEC402-E	BECCEC401R01-E			
	BECCEC404R01-E	BECDEC402-E	BECCEC401R01-E	BECCEC405R01-E	BECCEC405R01-E	BECCEC405R01-E		BECCEC402R01-E			
Tue				BECCEC406R01-E	BECCEC406R01-E	BECCEC406R01-E					
Wed		BECDEC401-E	BECCEC402R01-E	BECCEC401R01-E		BECCEC404R01-E	BECDEC402-E	BECCEC403R01-E	BECDEC401-E		
	BECCEC405R01-E	BECCEC405R01-E	BECCEC405R01-E	BECCEC403R01-E	BECDEC402-E		BECCEC401R01-E	BECDEC401-E			
Thu	BECCEC406R01-E	BECCEC406R01-E	BECCEC406R01-E								
		BECCEC403R01-E	BECCEC402R01-E	BECCEC404R01-E	BECCEC401R01-E		BECCEC405R01-E	BECCEC405R01-E	BECCEC405R01-E		
Fri							BECCEC406R01-E	BECCEC406R01-E	BECCEC406R01-E		
Sat											

Code	Description	Section	Faculty	Venue
BECCEC402R01	NETWORK THEORY	E	Narayanan, M	VV214, VIDHYUTH VIHAR
BECCEC403R01	LINEAR INTEGRATED CIRCUITS	E	Wilson, K J	VV214, VIDHYUTH VIHAR
BECCEC404R01	SIGNALS AND SYSTEMS	E	Parvathy, A	VV214, VIDHYUTH VIHAR
BECCEC405R01	CIRCUITS AND SYSTEM SIMULATION LAB	E	Ganapathy, R	LAB, VIDHYUTH VIHAR
BECCEC406R01	LINEAR INTEGRATED CIRCUITS LAB	E	Raajan, N R	VV214, VIDHYUTH VIHAR
BECCEC401R01	DISCRETE MATHEMATICS	E	Rajaraman, R	VV214, VIDHYUTH VIHAR
BECCTP407R01	HR SKILLS - II	E	Ravi, R	GNV313, GNANA VIHAR
BECDEC401	PULSE AND WAVE SHAPING CIRCUITS	E	Easwaran, M	VV214, VIDHYUTH VIHAR
BECDEC402	CONTROL ENGINEERING	E	Manigandan, N S	VV214, VIDHYUTH VIHAR